What is claimed is:

1. A multi-threading processor, comprising:

a front end module;

an execution module coupled to said front end module;

a state module coupled to said front end module and said execution module; and

a switch logic module coupled to said state module, wherein said switch logic module detects a mispredicted branch in a software thread and schedules a switch to another software thread during a latency of said mispredicted branch.

2. A multi-threading processor as recited in claim 1, wherein the switch logic module detects a switching event.

3. A multi-threading processor as recited in claim 2, wherein the switch logic module includes a mispredicted indicator that is set when a mispredicted branch is detected and reset when the switch is completed.

4. A multi-threading processor as recited in claim 3, wherein the switch logic module includes an outstanding switch request indicator that is set when the switching event does not require an immediate switch.

5. A multi-threading processor as recited in claim 4, wherein the switch logic module includes a counter to schedule a switch based on a time quantum.

6. A multi-threading processor as recited in claim 1, wherein the state module includes a pair of register files and a pair of IPs.

7. A multi-threading processor as recited in claim 6, wherein the IPs are coupled to the front end module and the register files are coupled to the execution module.

8. A method for concealing switch latency in a multi-threading processor, comprising:

detecting a switching event in a software thread;

determining whether a mispredicted branch has been detected in said software thread; and

executing a switch to another software thread during a latency of said mispredicted branch if said mispredicted branch has been detected.

9. A method for concealing switch latency in a multi-threading processor as recited in claim 8, further comprising executing a switch to another software thread if the switching event requires an immediate switch.

10. A method for concealing switch latency in a multi-threading processor as recited in claim 9, further comprising ensuring that the switch to another software thread is executed before a time quantum expires.

11. A method for concealing switch latency in a multi-threading processor as recited in claim 10, wherein the switch has a latency of about 15 to about 20 clocks.

12. A method for concealing switch latency in a multi-threading processor as recited in claim 11, wherein the time quantum is less than about 1,000 clocks.

13. A method for concealing switch latency in a multi-threading processor as recited in claim 12, wherein the time quantum is about 200 clocks.

14. A set of instructions residing in a storage medium, said set of instructions capable of being executed by a processor for searching data stored in a mass storage device comprising:

detecting a switching event in a software thread;

determining whether a mispredicted branch has been detected in said software thread; and

executing a switch to another software thread during a latency of said mispredicted branch if said mispredicted branch has been detected.

15. A method for concealing switch latency in a multi-threading processor as recited in claim 14, further comprising executing a switch to another software thread if the switching event requires an immediate switch.

16. A method for concealing switch latency in a multi-threading processor as recited in claim 15, further comprising ensuring that the switch to another software thread is executed before a time quantum expires.

17. A method for concealing switch latency in a multi-threading processor as recited in claim 16, wherein the switch has a latency of about 15 to about 20 clocks.

18. A method for concealing switch latency in a multi-threading processor as recited in claim 17, wherein the time quantum is less than about 1,000 clocks.

19. A method for concealing switch latency in a multi-threading processor as recited in claim 18, wherein the time quantum is about 200 clocks.